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(54) System and method of dual mode automatic gain control for a digital radio receiver

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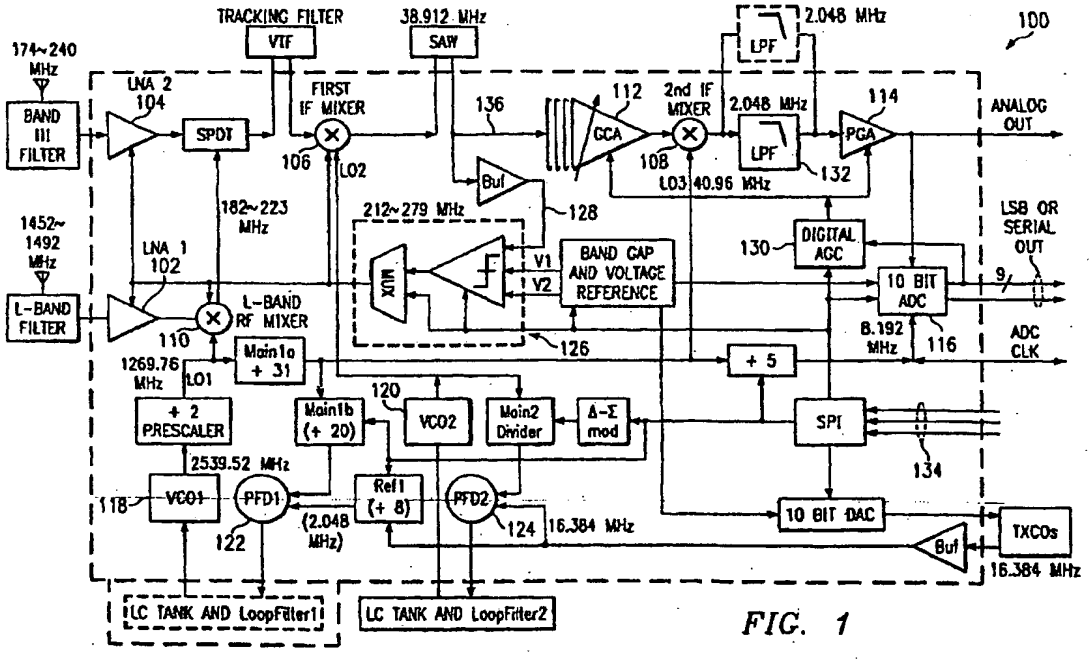

FIG. 1

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EUROPEAN SEARCH REPORT

Application Number
EP 02 10 0247

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.7)
X	EP 0 999 649 A (NOKIA MOBILE PHONES LTD) 10 May 2000 (2000-05-10) * paragraphs [0006] - [0024]; figures 1,3 *	1-7	H03G3/20
A	US 5 513 387 A (SAITO YUTAKA ET AL) 30 April 1996 (1996-04-30) * column 1, lines 34-58 * * column 2, line 41 - column 6, line 56 * * figures 1,4,11 *	1-7	
A	WO 00/18023 A (CONEXANT SYSTEMS INC) 30 March 2000 (2000-03-30) * page 2, line 19 - page 8, line 22 * * figure 1 *	1-7	
A	EP 0 913 934 A (SONY CORP) 6 May 1999 (1999-05-06) * paragraphs [0007], [0008], [0010] - [0058] * * figure 1 *	1-7	

TECHNICAL FIELDS SEARCHED (Int.Cl.7)
H03G
H04B

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
The Hague	26 April 2004	Goethals, F

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
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ANNEX TO THE EUROPEAN SEARCH REPORT ON EUROPEAN PATENT APPLICATION NO. EP 02 10 0247

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26-04-2004

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
EP 0999649 A	10-05-2000	FI 982409 A	07-05-2000
		EP 0999649 A2	10-05-2000
		US 2003045243 A1	06-03-2003
US 5513387 A	30-04-1996	JP 3254733 B2	12-02-2002
		JP 5347522 A	27-12-1993
WO 0018023 A	30-03-2000	US 6311048 B1	30-10-2001
		EP 1116337 A1	18-07-2001
		JP 2002525957 T	13-08-2002
		WO 0018023 A1	30-03-2000
EP 0913934 A	06-05-1999	JP 11136154 A	21-05-1999
		EP 0913934 A2	06-05-1999
		US 6226504 B1	01-05-2001

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For more details about this annex : see Official Journal of the European Patent Office, No. 12/82

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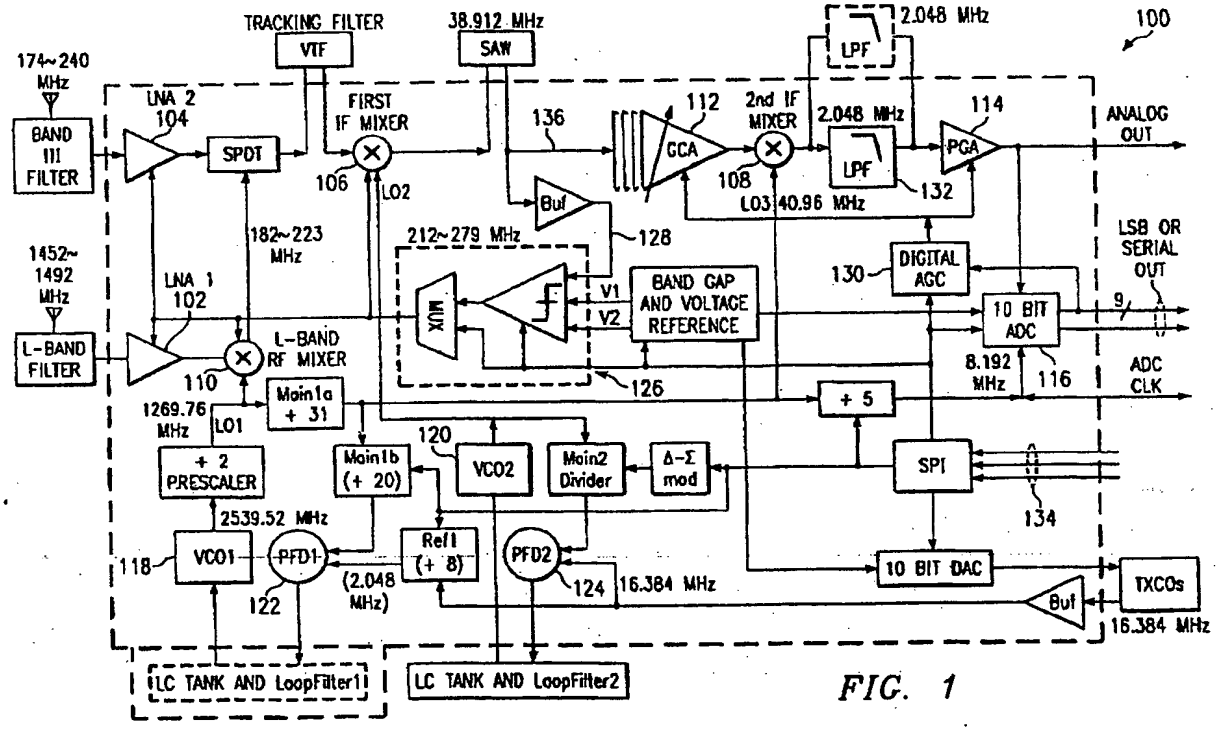

FIG. 1

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Description

Background of the Invention

1. Field of the Invention

[0001] This invention relates generally to automatic gain controls (AGC), and more particularly to a system and method of dual mode AGC for a digital radio receiver.

2. Description of the Prior Art

[0002] A digital radio broadcast system requires a radio frequency (RF) receiver having a high sensitivity and wide input dynamic range to cope with a wide range of RF input signal strengths. This requirement for a wide input dynamic range can only be met if the RF receiver has good linearity through the full RF receiver path over the required wide range of RF input signal strengths. The requirement to meet both high sensitivity and high linearity has been particularly problematic regarding RF receiver architectures and optimization.

[0003] In view of the foregoing, a need exists in the RF receiver art for an AGC architecture and method to optimize a digital radio receiver system such that it will achieve high input signal sensitivity and high linearity over a wide range of RF input signal strengths.

Summary of the Invention

[0004] The present invention is directed to a system architecture and method of implementing dual mode automatic gain control for a digital radio receiver in order to achieve high input signal sensitivity and high linearity over a wide range of RF input signal strengths. The architecture most preferably comprises a complete integrated RF dual band receiver solution for digital audio broadcast (DAB). According to one embodiment, the dual band receiver system architecture includes a pair of dual band low noise amplifiers (LNA), three down converters, an IF gain controlled amplifier (GCA), a programmable gain amplifier (PGA), a 10-bit analog-to-digital converter (ADC), two voltage controlled oscillators (VCO), and two synthesizers. In order to accommodate a wide range input signal (i.e. ~ -100 dBm to ~ -10 dBm) at both band III and L-band antennas, the LNAs and the first down converter mixers are designed with a two-mode architecture capable of implementing both high and low gain mode control, depending upon the strength of the input signal.

[0005] Two AGC control algorithms are implemented within the system to ensure a high system linearity and to obtain an optimum system signal-to-noise ratio for a wide range (i.e. ~ -100 dBm to ~ -10 dBm) of input signals. The high/low gain mode switches of LNAs and mixers are controlled by a RF AGC, while a digital AGC controls the gain settings of the GCA and PGA to optimize the output signal to the requisite ADC input range.

[0006] As used herein, the following words have the following meanings. The words "Algorithm" and "algorithmic" mean functions that can be implemented using either "hardware" or "software" or a combination of both. The words "algorithmic software" mean an algorithmic program used to direct the processing of data by a computer or data processing device. The words "data processing device" as used herein refer to a CPU, DSP, microprocessor, micro-controller, or other like device and an interface system. The interface system provides access to the data processing device such that data could be entered and processed by the data processing device. The words "discrete data" as used herein are interchangeable with "digitized data" and "digitized data" as used herein means data which are stored in the form of singularly isolated, discontinuous data or digits.

Brief Description of the Drawings

[0007] Other aspects and features of the present invention and many of the attendant advantages of the present invention will be readily appreciated as the same become better understood by reference to the following detailed description when considered in connection with the accompanying drawings in which like reference numerals designate like parts throughout the figures thereof and wherein:

Figure 1 is a block diagram illustrating a digital radio receiver with a dual mode automatic gain control system to achieve high input signal sensitivity and high linearity over a wide range of RF input signal strengths according to one embodiment of the present invention;

Figure 2 illustrates a single four-bit register for indicating gain status of the LNAs, mixers, GCA and PGA depicted in the digital radio receiver in Figure 1 where the MSB is the LNA bit, the second MSB is the mixer bit, the second LSB is the GCA bit, and the LSB is the PGA bit, according to one embodiment of the present invention;

Figure 3 illustrates four different states of the single four-bit register depicted in Figure 2 where the LSBs and MSBs are set to control four different gain modes (stages) according to one embodiment of the present invention;
Figure 4 is a state diagram illustrating the conditions necessary to implement a transition from one gain mode (stage) to another using the four different states of the single four-bit register depicted in Figure 3 according to one embodiment of the present invention;
Figure 5 is a flow chart illustrating an algorithmic procedure to identify stage status and implement gain decisions therefrom for the digital radio receiver depicted in Figure 1 and using the system features illustrated in Figures 2-4 according to one embodiment of the present invention;
Figure 6 is a flow chart illustrating an algorithmic procedure for implementing the stage I gain decision shown in Figure 5 according to one embodiment of the present invention;
Figure 7 is a flow chart illustrating an algorithmic procedure for implementing the stage II gain decision shown in Figure 5 according to one embodiment of the present invention;
Figure 8 is a flow chart illustrating an algorithmic procedure for implementing the stage III gain decision shown in Figure 5 according to one embodiment of the present invention; and
Figure 9 is a flow chart illustrating an algorithmic procedure for implementing the stage IV gain decision shown in Figure 5 according to one embodiment of the present invention.

[0008] While the above-identified drawing figures set forth alternative embodiments, other embodiments of the present invention are also contemplated, as noted in the discussion. In all cases, this disclosure presents illustrated embodiments of the present invention by way of representation and not limitation. Numerous other modifications and embodiments can be devised by those skilled in the art which fall within the scope and spirit of the principles of this invention.

Detailed Description of the Preferred Embodiments

[0009] Figure 1 is a block diagram illustrating a digital radio receiver 100 with a dual mode automatic gain control system to achieve high input signal sensitivity and high linearity over a wide range of RF input signal strengths according to one embodiment of the present invention. The digital radio receiver 100 includes a pair of dual band low noise amplifiers (LNAs) 102, 104, three down converters (mixers) 106, 108, 110, an IF gain controlled amplifier (CGA) 112, a programmable gain amplifier (GPA) 114, a 10-bit ADC 116, two VCOs 118, 120, and two synthesizers 122, 124. The LNAs 102, 104 and the first down converter mixers 106, 110 are implemented via a two-mode architecture having a high gain mode and a low gain mode control 126 that is dependent upon the strength of the input signal 128.
[0010] Two automatic gain control algorithms are implemented to ensure a high system 100 linearity and to obtain an optimum system 100 signal-to-noise ratio for a wide input signal range, as stated herein before. The high/low gain mode switches 126 of LNAs 102, 104 and mixers 106, 110 can be seen to be controlled by a RF AGC , while a digital AGC 130 controls the gain settings of GCA 112 and PGA 114 to optimize the PGA 114 output signal to ADC 116 input range.
[0011] Table I below shows four stages of gain control for the system 100 according to one preferred embodiment.

Table I

Pin (dBm)	GCA input (Vp-p)	Pout (Vp-p)	C/N (dB)	Control Stage
-100.00	0.00019	0.85	7.71	Stage I: LNA, Mixer
-90.00	0.00060	0.85	19.99	I: high gain
-82.00	0.00150	0.85	25.71	PGA=18 to ~ 0 (dB)
-81.00	0.00169	0.85	26.61	Stage II: LNA, Mixer
-57.00	0.02673	0.85	36.11	I: high gain
				PGA=0, GCA=39 to ~ 15 (dB)
-56.00	0.00300	0.85	35.85	Stage III: Mixer I:
-42.00	0.01503	0.85	36.24	low gain
-31.00	0.05334	0.85	36.25	LNA: high gain
				PGA=0, GCA=34 to ~ 9 (dB)
-30.00	0.00598	0.85	36.15	Stage IV: LNA, Mixer
-10.00	0.05985	0.85	36.25	I: low gain
				PGA=0, GCA=28 to ~ 8 (dB)

The present inventor discovered that positive channel fading effects on field strength must be considered. The output level of the LPF buffer 132 is therefore controlled to be 0.85 Vp-p, that is about -7.5 dB below the 2 Vp-p ADC 116 input range. The 0.85 Vp-p threshold is most preferably programmed in a fashion familiar to those skilled in the art of digital ADCs such that a real value of the threshold can be set when positive channel fading data becomes available, for example, from field tests.

[0012] The dual mode automatic gain control broadcast receiver system 100 most preferably does not allow any gain change within the RF chain during a packet (or symbol) receiving period. Instead, any gain change should be implemented during a packet (or symbol) interval period (e.g. 0.24 ms according to one embodiment). Such control can be achieved, for example, via a flag signal provided by a data processing unit such as a DSP. The flag signal could be presented, for example, at a dedicated DSP pin or could alternatively be presented to the receiver system 100 through its SPI bus 134 (if the SPI bus speed is fast enough).

[0013] The AGC 130 control can also be implemented using external data processing devices (e.g. DSP, micro-controller and the like). In this case, the internal AGC control loop is most preferably disabled through the SPI bus 134.

[0014] Table I shows that one embodiment of the present dual mode automatic gain control digital broadcast receiver 100 can be realized using four gain stages (I, II, III, IV) that are implemented with different combinations of four gain elements (LNA 102, 104, Mixer 106, GCA 112, PGA 114). Four 1-bit registers are therefore needed in the receiver system 100 to indicate the status of each gain block since only one LNA operates at any moment in time according to the present embodiment. Five one-bit registers would be necessary if the LNAs 102, 104 were allowed to function simultaneously. Figure 2 illustrates a single four-bit register 200 for indicating gain status of the LNAs 102, 104, mixer 106, GCA 112 and PGA 114 depicted in the digital radio receiver 100 shown in Figure 1, where the MSB 202 is the LNA bit, the second MSB 204 is the mixer bit, the second LSB 206 is the GCA bit, and the LSB 208 is the PGA bit, according to one embodiment of the present invention. This single four-bit register 200 is used to help implement an AGC control algorithm capable of controlling the receiver system 100 such that it can achieve high input signal sensitivity and high linearity over a wide range of RF input signal strengths as stated herein before. According to one embodiment, a "1" bit indicates a high gain status for both LNA and Mixer1, while a "0" bit indicates low gain status. Further, according to one embodiment, a "1" bit indicates a maximum gain of 40 dB for GCA 112, while a "0" bit indicates the GCA 112 gain can be adjustable between 0 ~ 40 dB. Regarding PGA 114, a "0" bit indicates a minimum gain of 0 dB while a "1" bit indicates PGA 114 gain can be adjustable between 0 ~ 18 dB, according to one embodiment. The AGC register value corresponding to stage I, II, III and IV respectively are shown in Figure 3 that illustrates four different states 302, 304, 306, 308 of the single four-bit register 200 depicted in Figure 2, where the LSBs 206, 208 and MSBs 202, 204 are set to control four different gain modes (stages) according to one embodiment of the present invention. The analog AGC is controlled by monitoring GCA 112 input signal 136 and the digital AGC 130 is controlled by monitoring ADC 116 output code, as stated herein before. With continued reference now to Table I, there are two threshold values of GCA input 136 to determine the change of either Mixer 106 gain or LNA 102, 104 gain. The threshold values are V1=26mV or V2=53mV for both L-band receive mode and Band III receive mode. For digital AGC, a setting of 0.85 Vp-p ADC input signal results in 730 digital code on ADC 116 output (1024 digital output code for 2 Vp-p ADC input).

[0015] Figure 4 is a state diagram 400 illustrating the conditions necessary to implement a transition from one gain mode (stage) to another using the four different states 302, 304, 306, 308 of the single four-bit register 200 depicted in Figure 3 according to one embodiment of the present invention. It can be seen that most transitions occur between two stages. There is a possible transition, however, from stage 1111 to stage 1000 as well as from stage 1111 to stage 1100, when the input signal strength increases dramatically. The present inventor found that identifying the current state of the stage to be most important among the receiver system 100 variables, since it can be determined which gain needs to be adjusted in order to optimize the receiver system 100 so long as the status of the stage is known.

[0016] Figure 5 is a flow chart illustrating an algorithmic procedure 500 to identify stage status and implement gain decisions therefrom for the digital radio receiver 100 depicted in Figure 1 and using the system features illustrated in Figures 2-4 according to one embodiment of the present invention. The algorithmic procedure 500 determines the AGC register 200 value of L, M, G and P to selectively implement a stage I, II, III or IV gain decision. As shown in Figure 5, after the stage I, II, II, IV status is identified, a respective Gain Decision I, II, III, IV algorithm is implemented. The Gain Decision algorithms determine which gain stages of receiver system 100 need to be adjusted, based on the GCA 112 input signal 136 strength and the ADC 116 output code. After the Gain Decision algorithms determine which gain stages need to be adjusted, the gain update is not immediately implemented. Instead, the gain update will wait on the Flag signal 502, that is controlled by the data processing device (e.g. DSP, micro-controller, or other like device). According to one embodiment, the Flag signal 502 is active low; so the gain is updated when Flag signal 502 is low.

[0017] With continued reference now to Figure 5, following an initial reset of the AGC register 200 as shown in block 504, a determination is first made regarding the status of the GCA register 206 as shown in block 506. If the GCA register 206 has its bit set at "1", a stage I Gain Decision algorithm is implemented as shown in blocks 508 and 510. If the GCA register 206 has its bit set at "0", a determination is then made regarding the status of the Mixer register 204 as shown in block 512. If the Mixer register 204 has its bit set at "1", a stage II Gain Decision algorithm is imple-

mented as shown in blocks 514 and 516. If the Mixer register 204 has its bit set at "0", a determination is then made regarding the status of the LNA register 202 as shown in block 518. If the LNA register 202 has its bit set at "1", a stage III Gain Decision algorithm is implemented as shown in blocks 520 and 522. If the LNA register 202 has its bit set at "0", a stage IV Gain Decision algorithm is then implemented as shown in blocks 524 and 526. Each selected Gain Decision algorithm proceeds to perform a gain update for a respective portion of the receiver system 100 followed by a Gain Register 200 update, as shown in block 530.

[0018] Figure 6 is a flow chart illustrating an algorithmic procedure 600 for implementing the stage I Gain Decision 510 shown in Figure 5 according to one embodiment of the present invention. An AGC register 200 having every bit set at "1" initiates a stage I Gain Decision since the GCA register 206 then has its bit also set at "1". The stage I Gain Decision algorithmic procedure then commences by first determining the GCA 112 input signal strength V as shown in block 602. If the GCA 112 input signal strength V is greater than V1 ± ΔV (hysteresis effects), then the Mixer 106 gain is set low, the GCA 112 gain is set to its maximum, and the PGA 114 gain is set to its minimum (M=0, G=0, P=0), as shown in block 604. This completes the transition from Stage I to Stage III, depicted as path 404 in Figure 4. If however, the GCA 112 input signal strength V is not greater the V1 ± ΔV, then the Mixer 106 gain is left unchanged (M=1) as shown in block 606; and a decision is made as to whether the ADC 116 output code is equal to, more than, or less than 730 ± Δ, as shown in block 608. If the ADC 116 output code is equal to 730 ± Δ, the PGA 114 gain remains unchanged (P=1, G=1) as shown in block 610. Otherwise the PGA 114 gain may be changed as shown as described herein below. The increment or decrement of PGA 114 gain can be a small gain step. It therefore requires several iterations to achieve a stable value. The PGA 114 gain value can actually be calculated as a ratio of difference between the ADC 116 output code and a target code (730 for the instant embodiment, for example) to the code value per 1 dB PGA 114 gain change. Any gain update must wait for the Flag signal 502 as stated herein before. With continued reference to Figure 6, it can be seen that if the ADC 116 output code is more than 730 ± Δ, a determination is than made as to whether the PGA 114 gain is at its minimum as shown in block 612. If the PGA 114 gain is at its minimum, then the PGA 114 gain is left unchanged (P=0, G=0), as shown in block 614. If however, the PGA 114 gain is not at its minimum, then it is reduced (P=1, G=1), as shown in block 616. If the ADC 116 output code is less than 730 ± Δ, as shown in block 608, then a determination is made as to whether the PGA 114 gain is set at its maximum as shown in block 618. If the PGA 114 gain is found to already be at its maximum, then the PGA 114 gain is left unchanged (P=1, G=1), as shown in block 610. If however, the PGA 114 gain is found to be less than its maximum, the PGA 114 gain is then adjusted to its maximum as shown in block 620. This completes the transition from Stage I to Stage II, depicted as path 402 in Figure 4. As shown in block 622, the LNA register 202 bit is always set at "1", while the remaining registers 204, 206, 208 are updated during a stage I Gain Decision 600.

[0019] Figure 7 is a flow chart illustrating an algorithmic procedure 700 for implementing the stage II Gain Decision shown in Figure 5 according to one embodiment of the present invention. An AGC register 200 having the L and M bits set at "1" and the G and P bits set at "0", initiates a stage II Gain Decision. As stated herein before, the analog AGC is controlled by monitoring the GCA 112 input signal and the digital AGC 130 is controlled by monitoring the ADC 116 output code. As shown in Table I, there are two threshold values of GCA 112 input signal to determine the change of either Mixer 106 gain or LNA 102, 104 gain. The threshold values are V1=26 mV or V2=53 mV for both L-Band receive mode and Band III receive mode. The stage II Gain Decision algorithmic procedure 700 then commences by first determining the GCA 112 input signal strength V as shown in block 702. If the GCA 112 input signal strength V is greater than V1 ± ΔV, then the Mixer 106 gain is set low, the GCA 112 gain is set to 34, and the PGA 114 gain is set to its minimum (M=0, G=0, P=0), as shown in block 704. This completes the transition from stage II to stage III, depicted as path 408 in Figure 4. If however, the GCA 112 input signal strength V is not greater the V1 ± ΔV, then the Mixer 106 gain is left unchanged (M=1) as shown in block 706; and a decision is made as to whether the ADC 116 output code is equal to, more than, or less than 730 ± Δ, as shown in block 708. If the ADC 116 output code is equal to 730 ± Δ, the GCA 112 gain remains unchanged (G=0, P=0) as shown in block 710. Otherwise the GCA 112 gain may be changed as shown as described herein below. Stage II can transit to stage I (1111) for a weak input signal and to stage III (1000) for a strong input signal. The (1000) transition occurs when the GCA 112 input reaches V1 threshold value. The (1111) transition occurs when the GCA 112 gain reaches maximum value while the ADC 116 output code is still less than the targeted code (e.g. 730). Any gain update must wait for the Flag signal 502 as stated herein before. With continued reference to Figure 7, it can be seen that if the ADC 116 output code is more than 730 ± Δ, a determination is than made as to whether the GCA 112 gain is at its minimum as shown in block 712. If the GCA 112 gain is at its minimum, then the GCA 112 gain is left unchanged (G=0, P=0), as shown in block 710. If however, the GCA 112 gain is not at its minimum, then it is reduced (G=1, P=1), as shown in block 714. If the ADC 116 output code is less than 730 ± Δ, as shown in block 708, then a determination is made as to whether the GCA 112 gain is set at its maximum as shown in block 716. If the GCA 112 gain is found to already be at its maximum, then the GCA 112 gain is left unchanged (G=1, P=1), as shown in block 718. If however, the GCA 112 gain is found to be less than its maximum, the GCA 112 gain is then adjusted upward (G=0, P=0) as shown in block 720. This completes a transition from stage II to stage I, depicted as path 402 in Figure 4. As shown in block 722, the LNA register 202 bit is always set at "1", while the remaining

registers 204, 206, 208 are updated during a stage II Gain Decision 700.

[0020] Figure 8 is a flow chart illustrating an algorithmic procedure 800 for implementing the stage III Gain Decision shown in Figure 5 according to one embodiment of the present invention. An AGC register 200 having the L bits set at "1" and the M, G and P bits set at "0", initiates a stage III Gain Decision as seen in block 802. As stated herein before, the analog AGC is controlled by monitoring the GCA 112 input signal and the digital AGC 116 is controlled by monitoring the ADC 116 output code. As shown in Table I, there are two threshold values of GCA 112 input signal to determine the change of either Mixer 106 gain or LNA 102, 104 gain. The threshold values are V1=26 mV or V2=53 mV for both L-Band receive mode and Band III receive mode. The stage III Gain Decision algorithmic procedure 800 then commences by first determining the GCA 112 input signal strength V as shown in block 804. If the GCA 112 input signal strength V is greater than V2 ± ΔV, then the Mixer 106 gain is set low, the LNA 102, 104 gain is set low, the GCA 112 gain is set to 28, and the PGA 114 gain is set to its minimum (L=0, M=0, G=0, P=0), as shown in block 806. This completes the transition from stage III to stage IV, depicted as path 406 in Figure 4. If however, the GCA 112 input signal strength V is not greater the V2 ± ΔV, then the LNA 102, 104 gain is left unchanged (L=1) as shown in block 808; and a decision is made as to whether the ADC 116 output code is equal to, more than, or less than 730 ± Δ, as shown in block 810. If the ADC 116 output code is equal to 730 ± Δ, the GCA 112 gain remains unchanged (M=0, G=0, P=0) as shown in block 812. Otherwise the GCA 112 gain may be changed as shown as described herein below. Any gain update must wait for the Flag signal 502 as stated herein before. With continued reference to Figure 8, it can be seen that if the ADC 116 output code is more than 730 ± Δ, a determination is than made as to whether the GCA 112 gain is at its minimum as shown in block 814. If the GCA 112 gain is at its minimum, then the GCA 112 gain is left unchanged (M=0, G=0, P=0), as shown in block 812. If however, the GCA 112 gain is not at its minimum, then it is adjusted downward to its minimum (M=0, G=0, P=0), as shown in block 816. If the ADC 116 output code is less than 730 ± Δ, as shown in block 810, then a determination is made as to whether the GCA 112 gain is set at its maximum as shown in block 818. If the GCA 112 gain is found to already be at its maximum, then the GCA 112 gain is left unchanged (M=1, G=0, P=0), as shown in block 820. If however, the GCA 112 gain is found to be less than its maximum, the GCA 112 gain is then adjusted to its maximum (M=0, G=0, P=0) as shown in block 822. This completes a transition from stage III to stage II, depicted as path 408 in Figure 4. As shown in block 824, all registers 202, 204, 206, 208 are updated during a stage III Gain Decision 700.

[0021] Figure 9 is a flow chart illustrating an algorithmic procedure 900 for implementing the stage IV gain decision shown in Figure 5 according to one embodiment of the present invention. An AGC register 200 having the L, M, G and P bits set at "0", initiates a stage IV Gain Decision as seen in block 902. As stated herein before, the analog AGC is controlled by monitoring the GCA 112 input signal and the digital AGC 116 is controlled by monitoring the ADC 116 output code. As shown in Table I, there are two threshold values of GCA 112 input signal to determine the change of either Mixer 106 gain or LNA 102, 104 gain. The threshold values are V1=26 mV or V2=53 mV for both L-Band receive mode and Band III receive mode. The stage IV Gain Decision algorithmic procedure 900 commences by first determining whether the ADC 116 output code is equal to, more than, or less than 730 ± Δ, as shown in block 904. If the ADC 116 output code is equal to 730 ± Δ, the GCA 112 gain remains unchanged (M=0, G=0, P=0) as shown in block 906. Otherwise the GCA 112 gain may be changed as shown as described herein below. Any gain update must wait for the Flag signal 502 as stated herein before. With continued reference to Figure 9, it can be seen that if the ADC 116 output code is more than 730 ± Δ, a determination is than made as to whether the GCA 112 gain is at its minimum as shown in block 908. If the GCA 112 gain is at its minimum, then the GCA 112 gain is left unchanged (M=0, G=0, P=0), as shown in block 906. If however, the GCA 112 gain is not at its minimum, then it is adjusted downward to its minimum (M=0, G=0, P=0), as shown in block 910. If the ADC 116 output code is less than 730 ± Δ, as shown in block 810, then a determination is made as to whether the GCA 112 gain is set at its maximum as shown in block 912. If the GCA 112 gain is found to already be at its maximum, then the GCA 112 gain is set at a value of Max=20 dB and the LNA 102, 106 gain is set high (L=1, M=0, G=0, P=0), as shown in block 914. This completes the transition from stage IV to stage III, depicted as path 406 in Figure 4. If however, the GCA 112 gain is found to be less than its maximum, the GCA 112 gain is then adjusted to its maximum (M=0, G=0, P=0) as shown in block 916. As shown in block 918, all registers 202, 204, 206, 208 are updated during a stage IV Gain Decision 900.

[0022] In summary explanation of the above, the present invention is directed to digital radio receiver architecture 100 and an algorithmic technique 500, 600, 700, 800, 900 to achieve high input signal sensitivity and high linearity over a wide range of RF input signal strengths at both band III and L-band antennas, among other things. The technique uses algorithmic software to implement program-based automatic gain control to ensure and obtain an optimum system signal-to-noise ratio. High/low gain mode switches associated with LNAs 102, 104 and mixers 106, 108, 110 are controlled by a RF AGC, while a digital AGC 130 controls the gain settings of a GCA 112 and a PGA 114 to optimize the PGA 114 output signal to a desired ADC 116 input range.

[0023] This invention has been described in considerable detail in order to provide those skilled in the equalizer art with the information needed to apply the novel principles and to construct and use such specialized components as are required. In view of the foregoing descriptions, it should be apparent that the present invention represents a sig-

nificant departure from the prior art in construction and operation. However, while particular embodiments of the present invention have been described herein in detail, it is to be understood that various alterations, modifications and substitutions can be made therein without departing in any way from the spirit and scope of the present invention, as defined in the claims which follow.

Claims

1. A method of implementing dual mode automatic gain control for a digital radio receiver, the method comprising the steps of:

   (a) providing a RF broadcast receiver having an IF gain controlled amplifier (GCA), a programmable gain amplifier (PGA), a digital automatic gain control (AGC) configured to control GCA gain and PGA gain in response to at least a digital output code that is determined partially by PGA output signal strength, at least one low noise amplifier (LNA), at least one down converter (Mixer), and an analog AGC configured to control LNA gain and Mixer gain in response to at least a GCA input signal;
   (b) providing a gain control register having a LNA control bit, a Mixer control bit, a GCA control bit, and a PGA control bit;
   (c) resetting the gain control register bits to an initial state; and
   (d) adjusting LNA gain and Mixer gain via the analog AGC in response to the control register bit setting and the GCA input signal and further adjusting GCA gain and PGA gain via the digital AGC in response to the control register bit setting and the digital output code such that the LNA gain, Mixer gain, GCA gain and PGA gain combine to render the RF broadcast receiver capable of maximizing its signal-to-noise ratio and linearity to accommodate reception and amplification of L-band signals and band-III signals.

2. The method of implementing dual mode automatic gain control for a digital radio receiver according to claim 1 further comprising the steps of:

   (e) adjusting the gain control register bits to a state determined by LNA gain, Mixer gain, GCA gain and PGA gain; and
   (f) repeating steps (d) and (e) for a desired period of time.

3. The method of implementing dual mode automatic gain control according to claim 1 or claim 2 wherein the step (d) of adjusting LNA gain, Mixer gain, GCA gain and PGA gain further comprises the steps of:

   implementing a first algorithmic gain decision procedure when the gain control register bits are all set to one;
   implementing a second algorithmic gain decision procedure when the gain control register LNA and Mixer bits are set to one and the gain control register GCA and PGA bits are set to zero;
   implementing a third algorithmic gain decision procedure when the gain control register LNA bit is set to one and the gain control register Mixer, GCA and PGA bits are set to zero; and
   implementing a fourth algorithmic gain decision procedure when the gain control register bits are all set to zero.

4. A digital radio receiver comprising:

   a IF gain controlled amplifier (GCA) having a variable gain;
   a programmable gain amplifier (PGA) having a variable gain;
   at least one low noise amplifier (LNA) having a variable gain;
   at least one down converter (Mixer) having a variable gain;
   a digital automatic gain control (AGC); and
   a gain control register bit map having a GCA control bit, a PGA control bit, a LNA control bit, and a Mixer control bit, wherein the AGC is responsive to the gain control register bit map to enable a plurality of AGC states such that the digital radio receiver can maximize its signal-to-noise ratio and linearity to accommodate reception and amplification of L-band signals and band-III signals.

5. The digital radio receiver according to claim 4 wherein the plurality of AGC states is determined in response to the PGA gain, the LNA gain, the Mixer gain and the AGC gain.

6. The digital radio receiver according to claim 4 or claim 5 wherein the plurality of AGC states comprise:

a first gain stage when the gain control register bits are all set to a first state;
a second gain stage when the gain control register bits are all set to a second state;
a third gain stage when the gain control register bits are all set to a third state; and
a fourth gain stage when the gain control register bits are all set to a fourth state.

7. The digital radio receiver according to claim 6 wherein the first state is implemented when the gain control register bits are all set to one, the second state is implemented when the gain control register LNA and Mixer bits are set to one and the gain control register GCA and PGA bits are set of zero, the third state is implemented when the gain control register LNA bit is set to one and the gain control register Mixer, GCA and PGA bits are set to zero, and the fourth state is implemented when the gain control register bits are all set to zero.

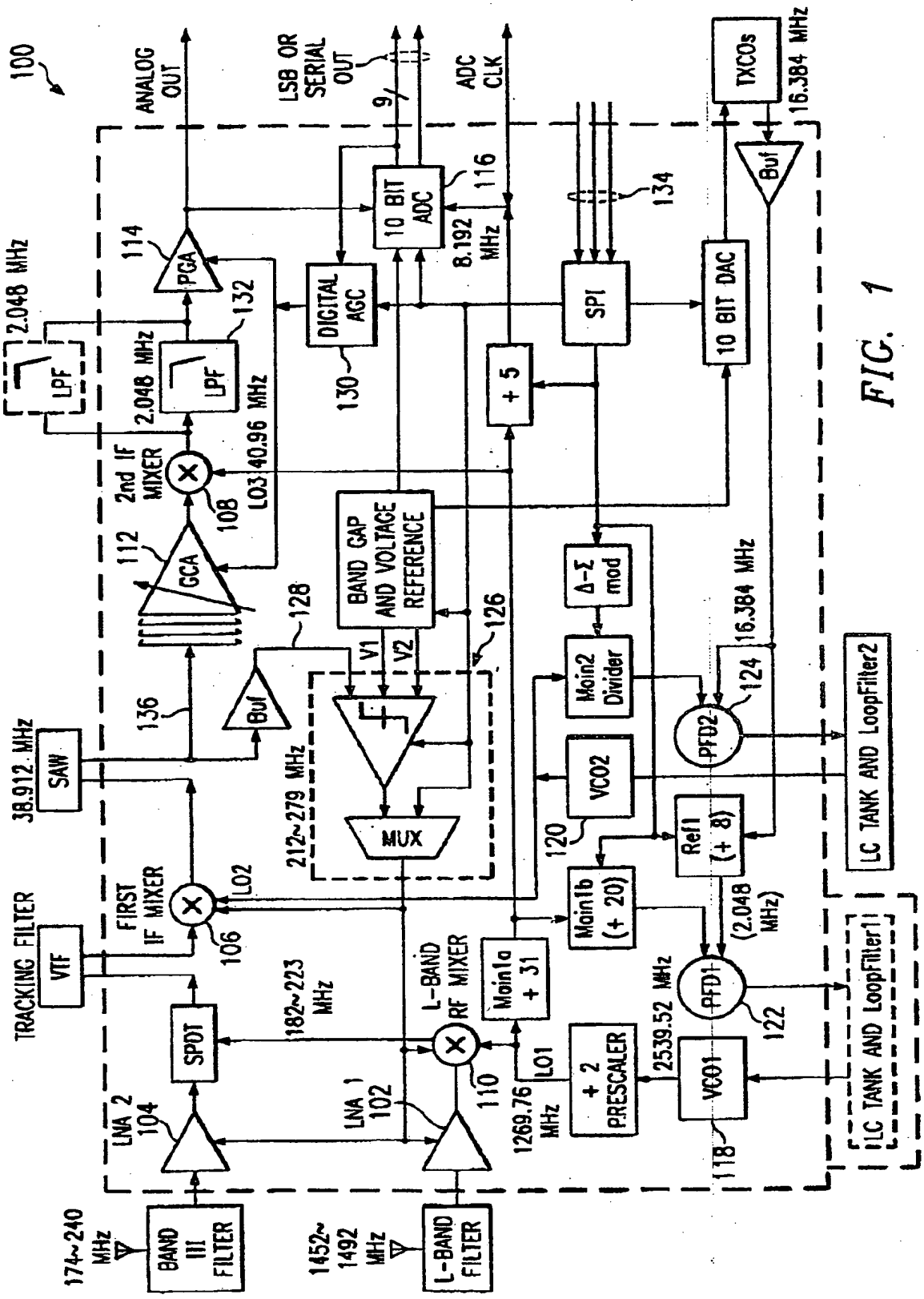
100
ANALOG OUT
LSB OR SERIAL OUT
9
ADC CLK
TXCOs
16.384 MHz
Buf
10 BIT ADC
116
8.192 MHz
134
SPI
10 BIT DAC
114
PGA
132
DIGITAL AGC
130
2.048 MHz
LPF
2.048 MHz
LPF
+ 5
2nd IF MIXER
LO3
40.96 MHz
108
112
GCA
BAND GAP AND VOLTAGE REFERENCE
128
126
V1
V2
Δ-Σ mod
Main2 Divider
16.384 MHz
124
PFD2
VCO2
120
Ref1 (÷ 8)
LC TANK AND LoopFilter2
38.912 MHz
SAW
136
Buf
MUX
212~279 MHz
TRACKING FILTER
VTF
FIRST IF MIXER
LO2
106
Main1b (÷ 20)
(2.048 MHz)
182~223 MHz
L-BAND RF MIXER
Main1a ÷ 31
SPDT
LO1
2539.52 MHz
PFD1
122
LC TANK AND LoopFilter1
LNA 2
104
LNA 1
102
110
1269.76 MHz
÷ 2 PRESCALER
VCO1
118
174~240 MHz
BAND III FILTER
1452~1492 MHz
L-BAND FILTER

FIG. 1

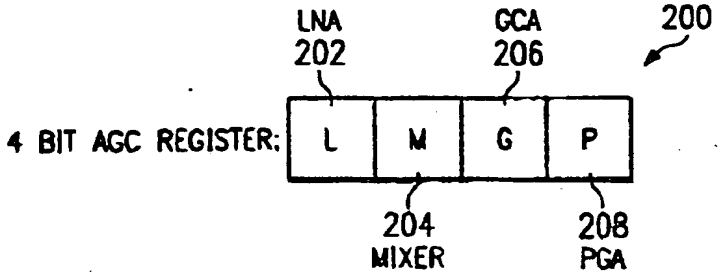

FIG. 2

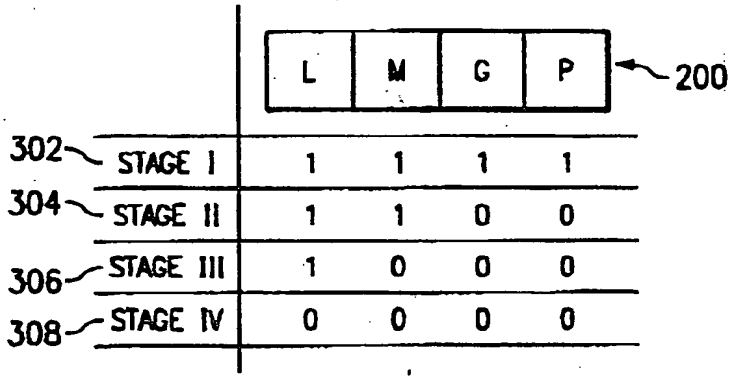

FIG. 3

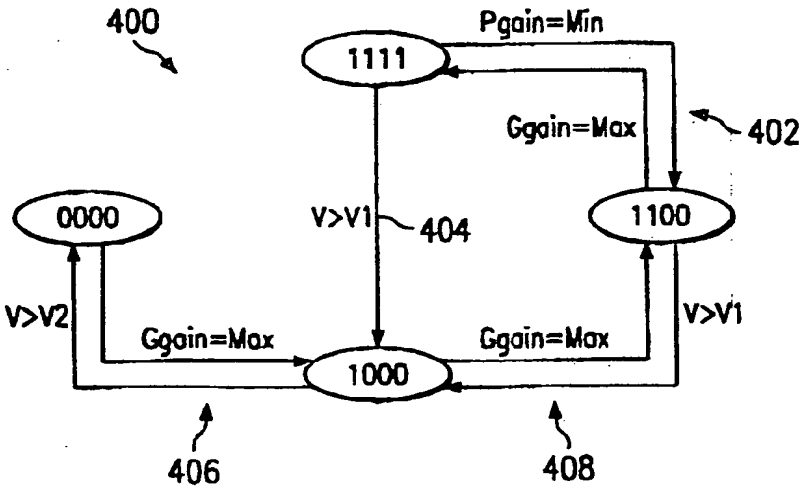

FIG. 4

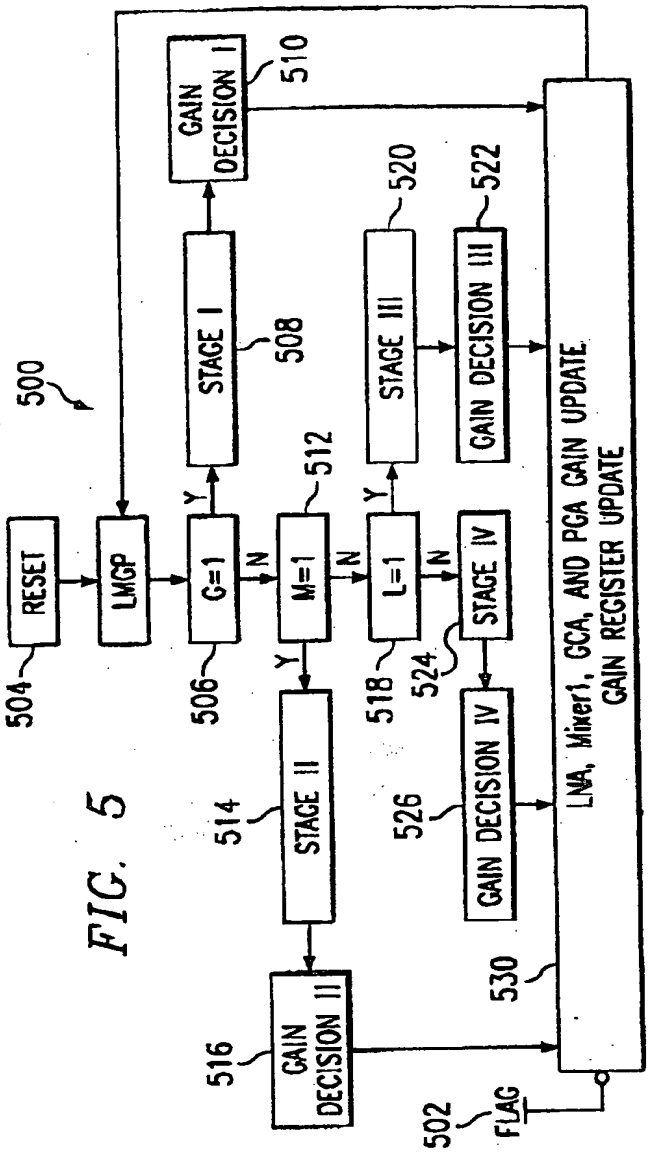
500
RESET
504
LMGP
G=1
506
M=1
512
L=1
518
STAGE IV
524
STAGE I
508
STAGE II
514
STAGE III
520
STAGE IV
522
GAIN DECISION I
510
GAIN DECISION II
516
GAIN DECISION III
GAIN DECISION IV
526
LNA, Mixer1, GCA, AND PGA GAIN UPDATE
GAIN REGISTER UPDATE
530
FLAG
502
Y
N

FIG. 5

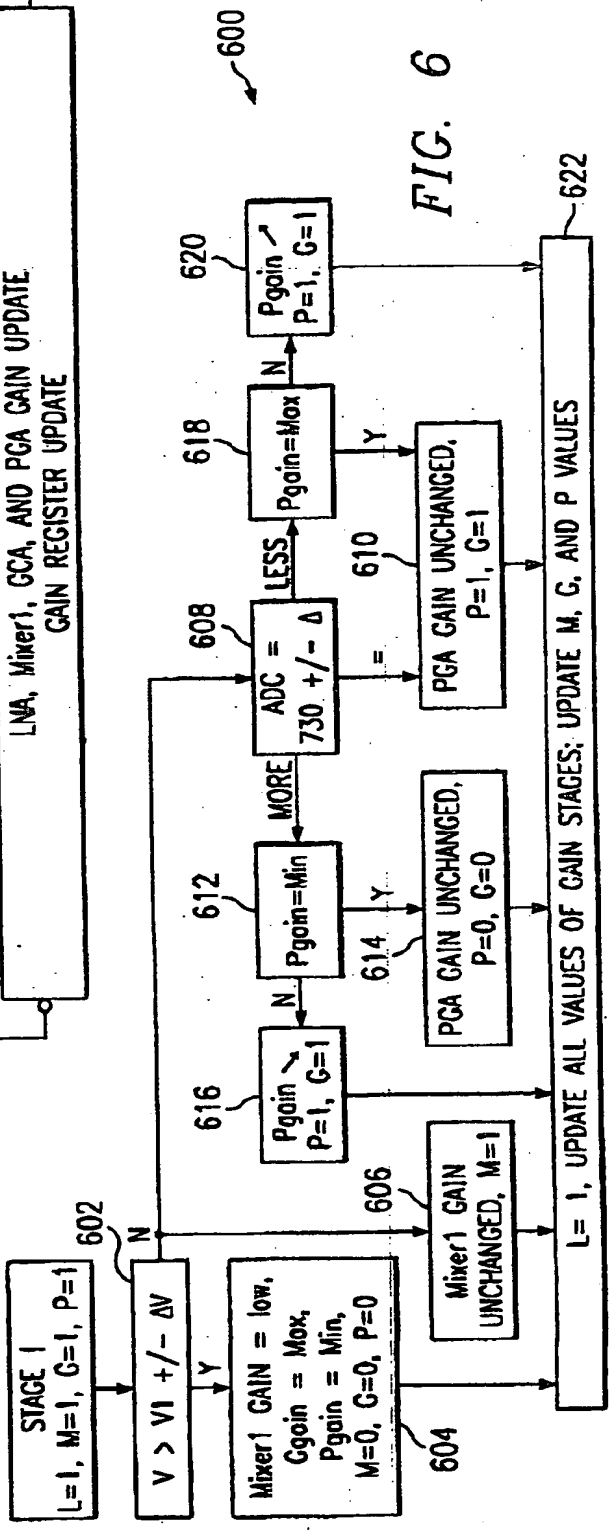
600
STAGE I
L=1, M=1, G=1, P=1
602
V > V1 +/- ΔV
Mixer1 GAIN = low,
Cgain = Max,
Pgain = Min,
M=0, G=0, P=0
604
Mixer1 GAIN
UNCHANGED, M=1
606
L= 1, UPDATE ALL VALUES OF GAIN STAGES; UPDATE M, G, AND P VALUES
622
Pgain
P=1, G=1
616
Pgain=Min
612
PGA GAIN UNCHANGED,
P=0, G=0
614
ADC =
730 +/- Δ
608
MORE
LESS
=
Pgain=Max
618
PGA GAIN UNCHANGED,
P=1, G=1
610
Pgain
P=1, G=1
620
Y
N

FIG. 6

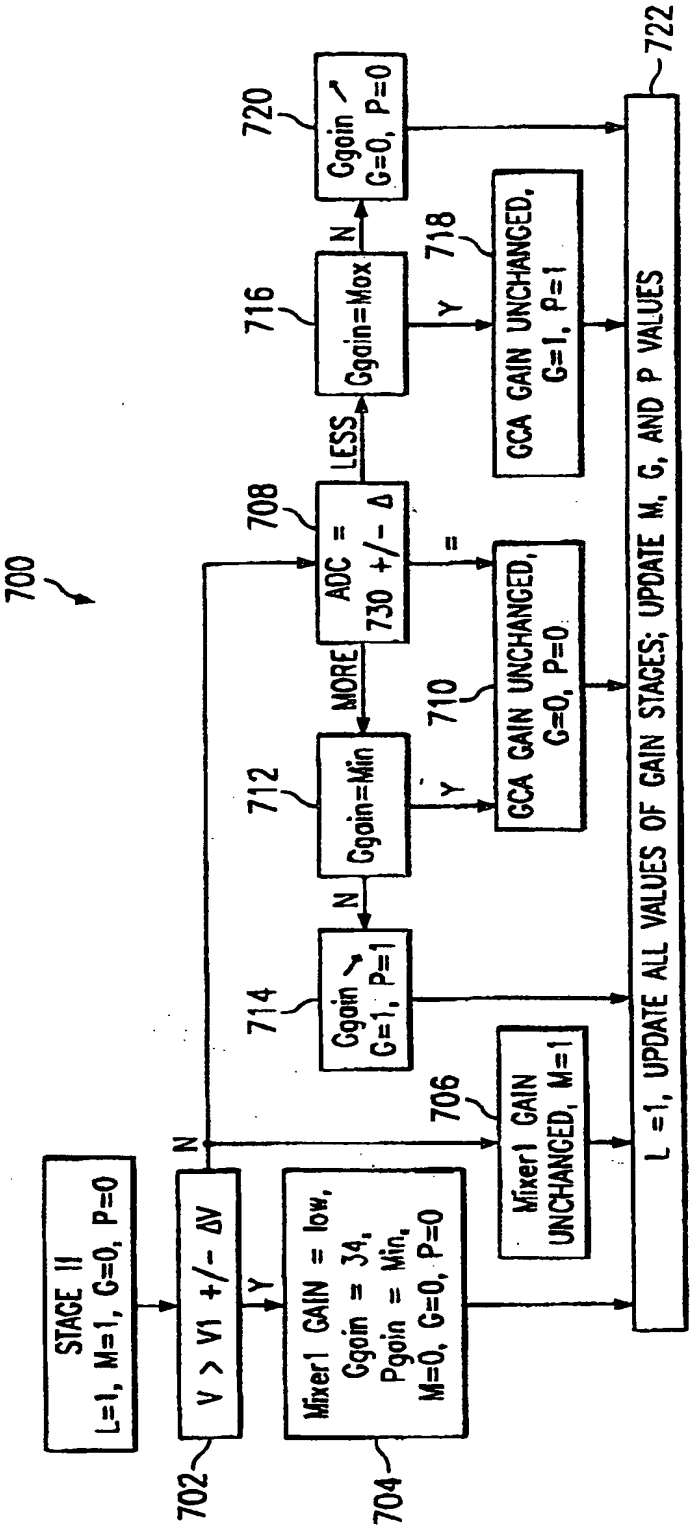
700
STAGE II
L=1, M=1, G=0, P=0
V > V1 +/- ΔV
N
Y
702
Mixer1 GAIN = low,
Ggain = 34,
Pgain = Min,
M=0, G=0, P=0
704
Mixer1 GAIN
UNCHANGED, M=1
706
ADC =
730 +/- Δ
MORE
=
LESS
708
Ggain=Min
712
Y
GCA GAIN UNCHANGED,
G=0, P=0
710
N
Ggain
G=1, P=1
714
Ggain=Mox
716
Y
GCA GAIN UNCHANGED,
G=1, P=1
718
N
Ggain
G=0, P=0
720
L =1, UPDATE ALL VALUES OF GAIN STAGES; UPDATE M, G, AND P VALUES
722

FIG. 7

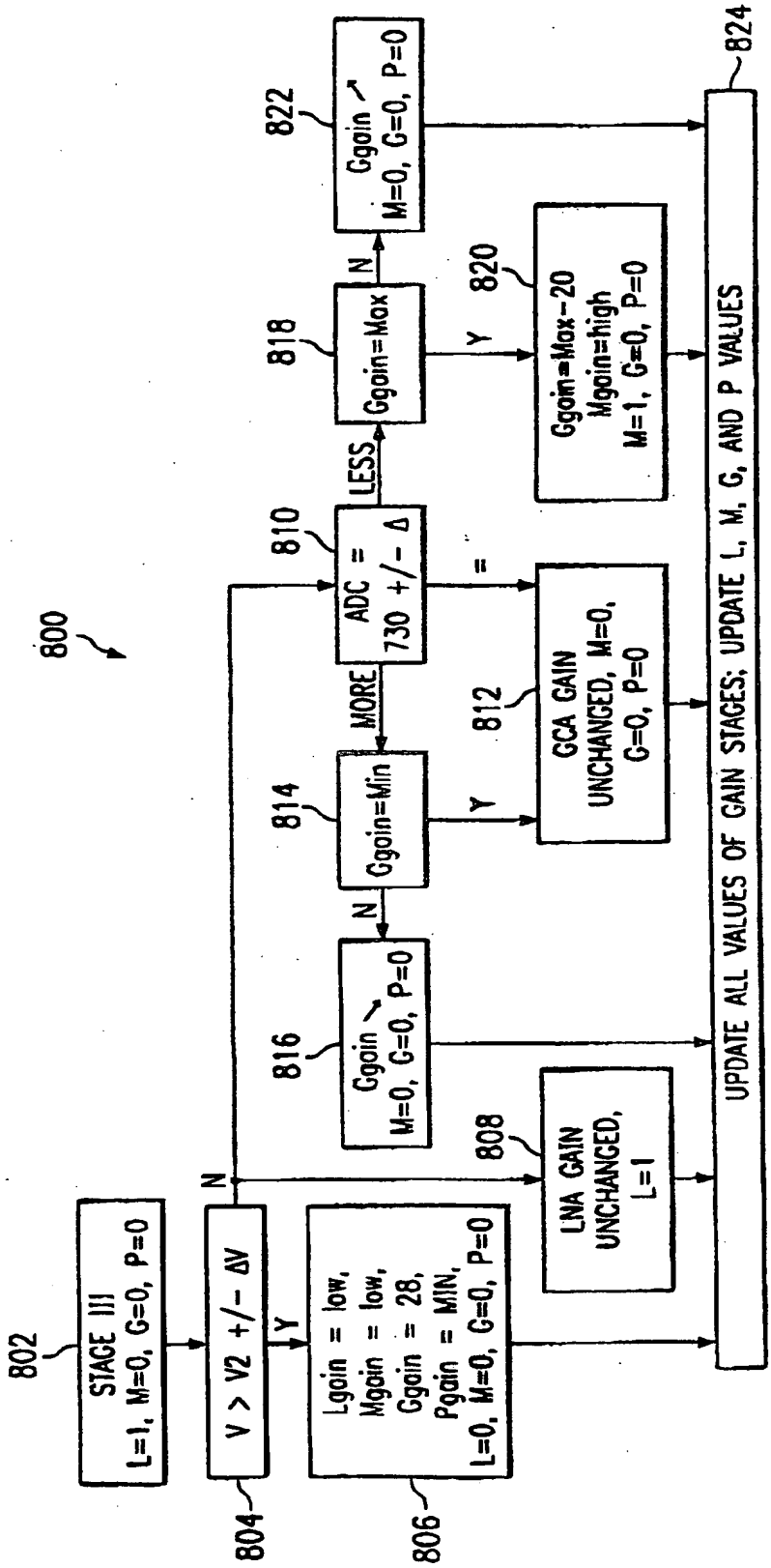
800
802
STAGE III
L=1, M=0, G=0, P=0
804
V > V2 +/- ΔV
Y
N
806
Lgain = low,
Mgain = low,
Ggain = 28,
Pgain = MIN,
L=0, M=0, G=0, P=0
808
LNA GAIN
UNCHANGED,
L=1
810
ADC =
730 +/- Δ
LESS
MORE
=
812
GCA GAIN
UNCHANGED, M=0,
G=0, P=0
814
Ggain=Min
Y
N
816
Ggain
M=0, G=0, P=0
818
Ggain=Max
Y
N
820
Ggain=Max-20
Mgain=high
M=1, G=0, P=0
822
Ggain
M=0, G=0, P=0
824
UPDATE ALL VALUES OF GAIN STAGES; UPDATE L, M, G, AND P VALUES

FIG. 8

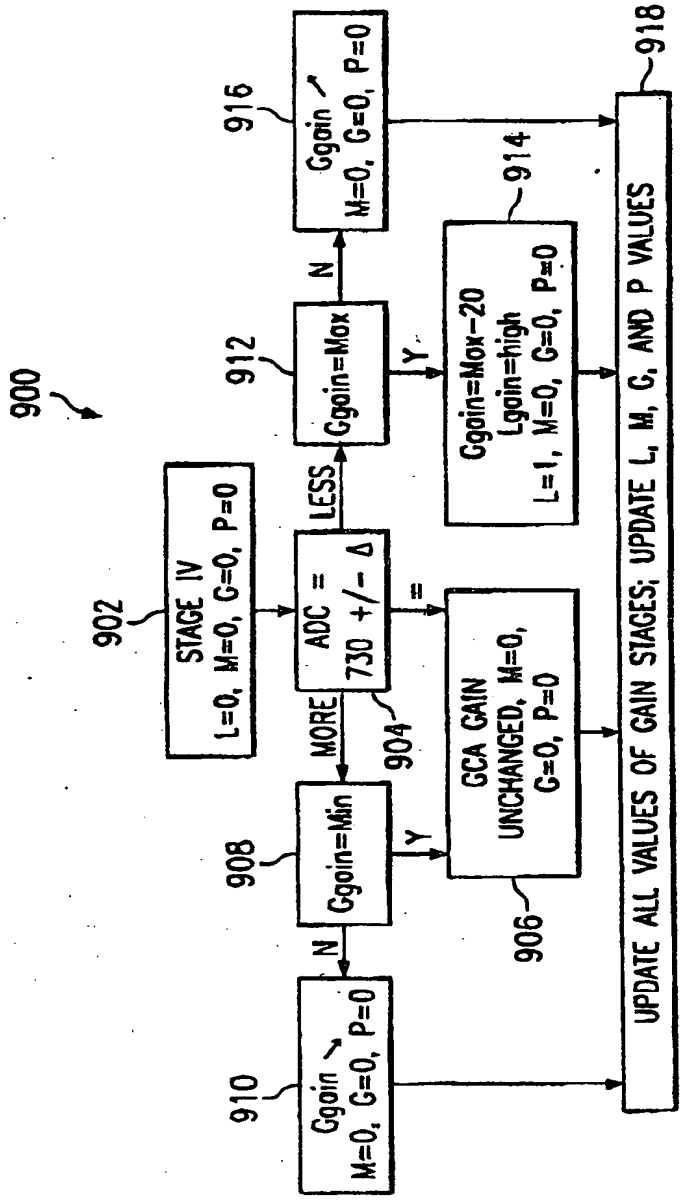
900
902
STAGE IV
L=0, M=0, G=0, P=0
904
ADC = 730 +/- Δ
MORE
LESS
=
906
GCA GAIN UNCHANGED, M=0, G=0, P=0
908
Ggain=Min
Y
N
910
Ggain
M=0, G=0, P=0
912
Ggain=Max
Y
N
914
Ggain=Max-20
Lgain=high
L=1, M=0, G=0, P=0
916
Ggain
M=0, G=0, P=0
918
UPDATE ALL VALUES OF GAIN STAGES; UPDATE L, M, G, AND P VALUES

FIG. 9